Recent Measurements of FE-B

K. Einsweiler and J. Richardson LBNL

Summarize measurements over last few months of FE-B:

- Single chip characterization
- Module characterization

Single Chip Characterization

Have now built 29 single-chip assemblies. Trying to characterize all of these devices in a consistent way, and account for everything. Now 11 of them have been in H8.

- Initial Boeing parts (CIS-1M = C1-01S, CIS-2M = C1-11D, Seiko = S1-21S)

  SPP-01 (Seiko): Cannot deplete detector, but electronics OK

  SCP-01 (Seiko): Detector OK, but noisy (500e). studied in June H8

  SCP-01 (CIS 2M): Detector OK, problems with analog injection

  S8O-01 (Seiko): Detector draws large current, very noisy

  S8O-01 (CIS-1M): Detector OK, noisy (500e), studied in June H8

  SBR-01 (CIS-2M): Detector OK, studied in June and Aug H8

- Initial IZM parts (CIS-1M = C1-05S, Seiko = S1-16S)

  ST1-01 (CIS-1M): Detector OK, good performance, studied in Aug H8

  ST2-02 (CIS-1M): Detector OK, good performance, some bad channels, studied in June and Aug H8

  SSG-01 (CIS-1M): Detector OK, good performance, studied in Aug H8

  S7O-01 (CIS-1M): Detector OK, good performance, studied in Aug H8

  ST1-01 (Seiko): Detector OK, noisy with many dead and unconnected channels

  SSG-01 (Seiko): Detector OK, chip produces no data

- Irradiated Boeing parts (fluence is 55 MeV p):

  ST1-02 (CIS-1M) 2.5×10^{14} : Detector OK, very noisy except at low bias, studied in Aug H8

  ST2-02 (CIS-1M) 2.5×10^{14}: Detector OK, good performance, studied in Aug H8

  ST1-02 (CIS-2M) 5.0×10^{14}: Detector OK, very noisy except at low bias, studied in Aug H8

  SCP-01 (CIS-1M) 2.6×10^{14}: Not tested

  SCP-02 (CIS-2M) 2.4×10^{14}: Not Tested

  ST2-02 (CIS-2M) 4.9×10^{14}: Detector OK, good performance, studied in Aug H8

  ST2-03 (CIS-2M) 2.5×10^{14}: Not Tested

- New Boeing parts

  SXT-02 (CIS-1M): Detector OK, electronics fine, sensitive to after-pulsing

  SSG-01 (CIS-1M): Detector OK, analog injection efficiency problems

  S7O-01 (CIS-1M): Detector OK, electronics fine

  S8O-01 (CIS-2M): Electronics OK digitally, detector draws no current, not photosensitive

- New IZM parts

  ST1-01 (CIS SiON): Not Tested

  ST1-02 (CIS SiON): Not Tested

  ST1-03 (CIS SiON): Not Tested

  ST2-01 (CIS SiON): Detector OK, electronics fine

  ST2-02 (CIS SiON): Detector OK, electronics fine

  ST2-03 (CIS SiON): Detector OK, electronics fine

Define basic set of measurements to characterize device:

- Basic electrical tests of chip (register tests and digital injection test)
- Threshold scan before/after TDAC tuning, also providing a list of bad channels
- TOT calibration with associated 3 parameter fit and fit status for each pixel
- I/V curve for detector
- Cd109 Source run, including gain calibration and list of dead channels

Test Beam needs:

- For different configurations used in testbeam (different DAC settings, leakage currents and HV biasses), carry out threshold scan and TOT calibration.
- Work now essentially complete for 33 different configurations used for 9 chips tested in Aug. H8 (soon to appear on relevant web pages).

Much work still to be done for overall studies:

- Some devices not yet tested beyond basic electronics tests. So far, only 1 chip of 29 fails the basic register/digital inject tests (not yet fully investigated).
- Record I/V curves for each assembly and make comparison with detector wafer probe data. See many but not all Tile 2 assemblies with much higher bias current than expected (although they work properly).
- See several chips with many bad channels, both for analog injection and for source run, but not for digital injection (from both bump vendors). Single channel failure mode due to components under input bond pad ?
- Different chips suffer from different levels of noise and after-pulsing, related to detector in some way. Look for correlations between detector design and vendor, after-pulsing, and noise levels. Do more systematic study of afterpulsing (dependence on number of pixels injected, charge injected, etc.) for those chips that show effects.

Other studies to be done:

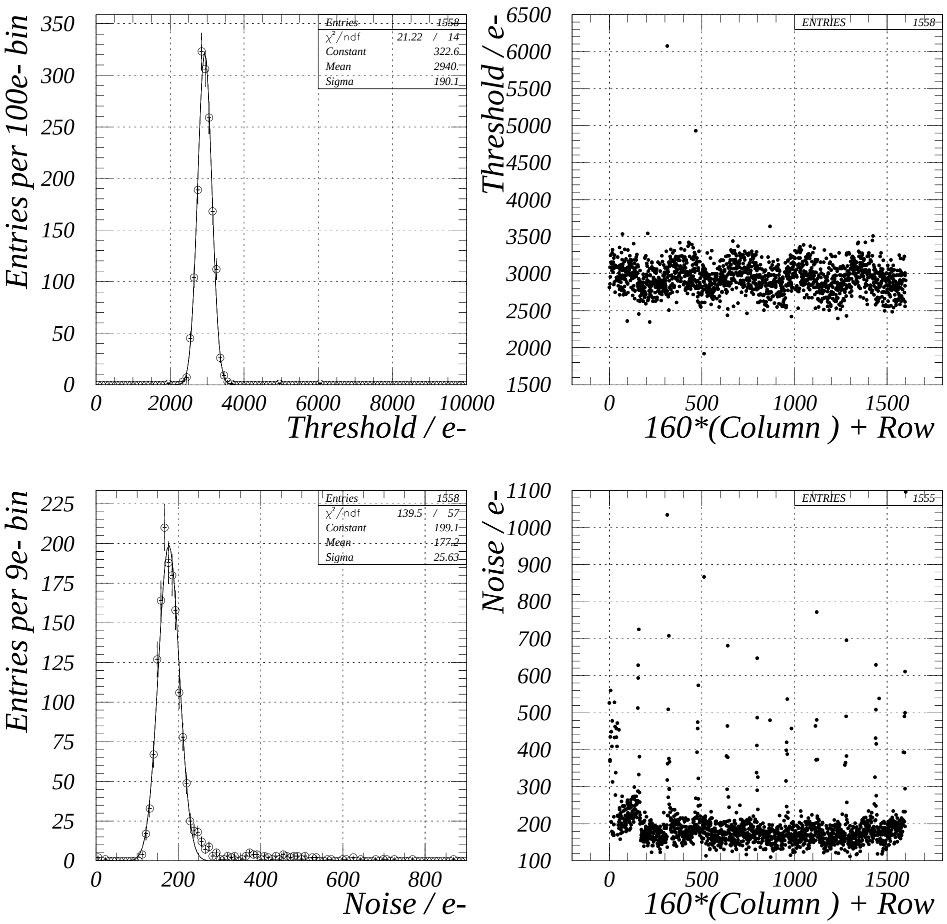
- Make cross-talk measurements with different detectors
- Do further studies of minimal decoupling required on support card
- Make more careful studies of cold electronics (have seen some apparent digital timing errors when running below -20 C ?)
- Do more “colliding beam mode” studies using TFIFO (make sure array performance is not disturbed by previously injected hits, etc.)

Some examples of interesting measurements

Threshold scans:

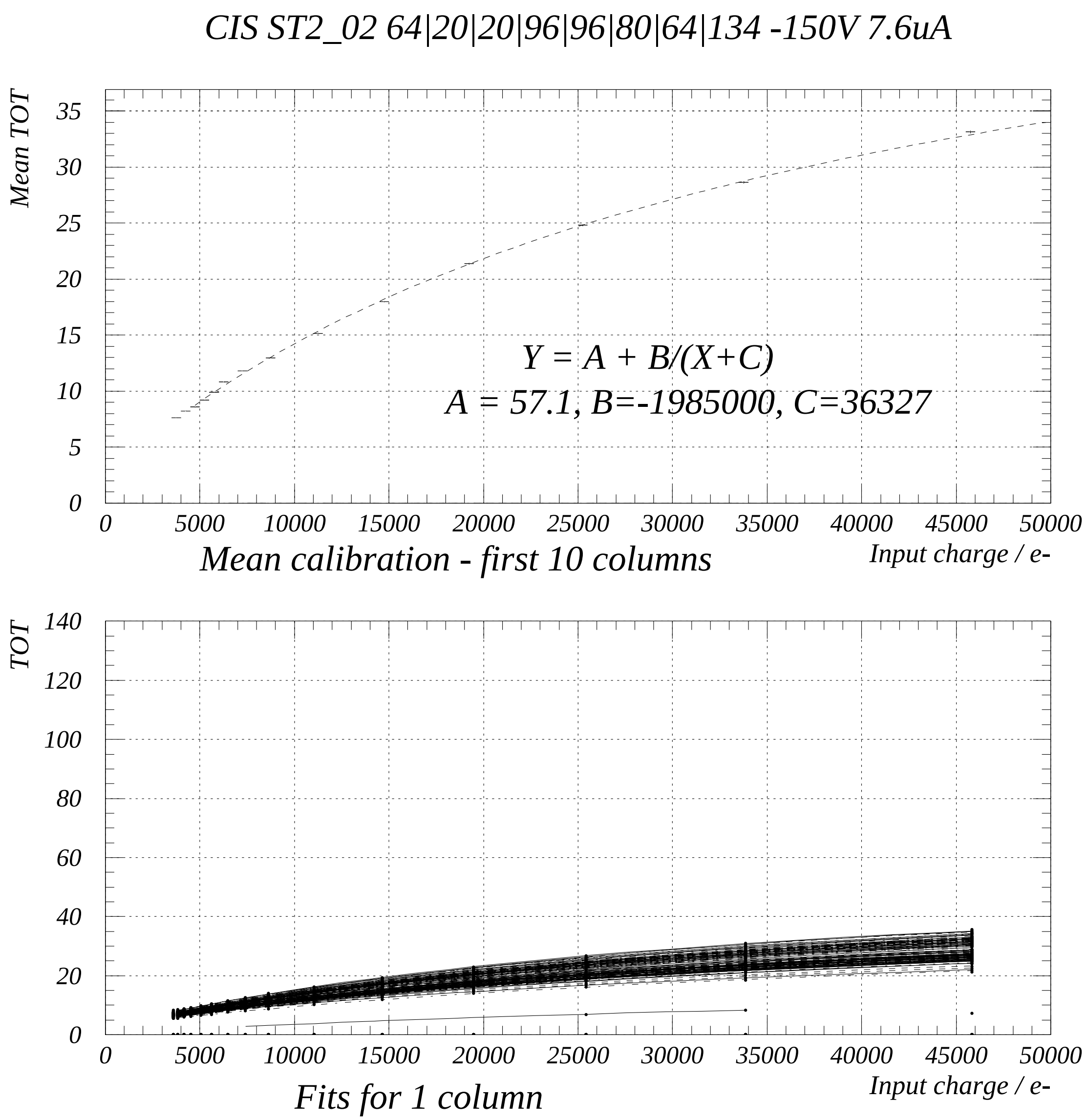
- Standard threshold and feedback current scan for an ST2:

CIS ST2_02 64/20/20/96/96/80/64/134 tuned 150V 7.6uA



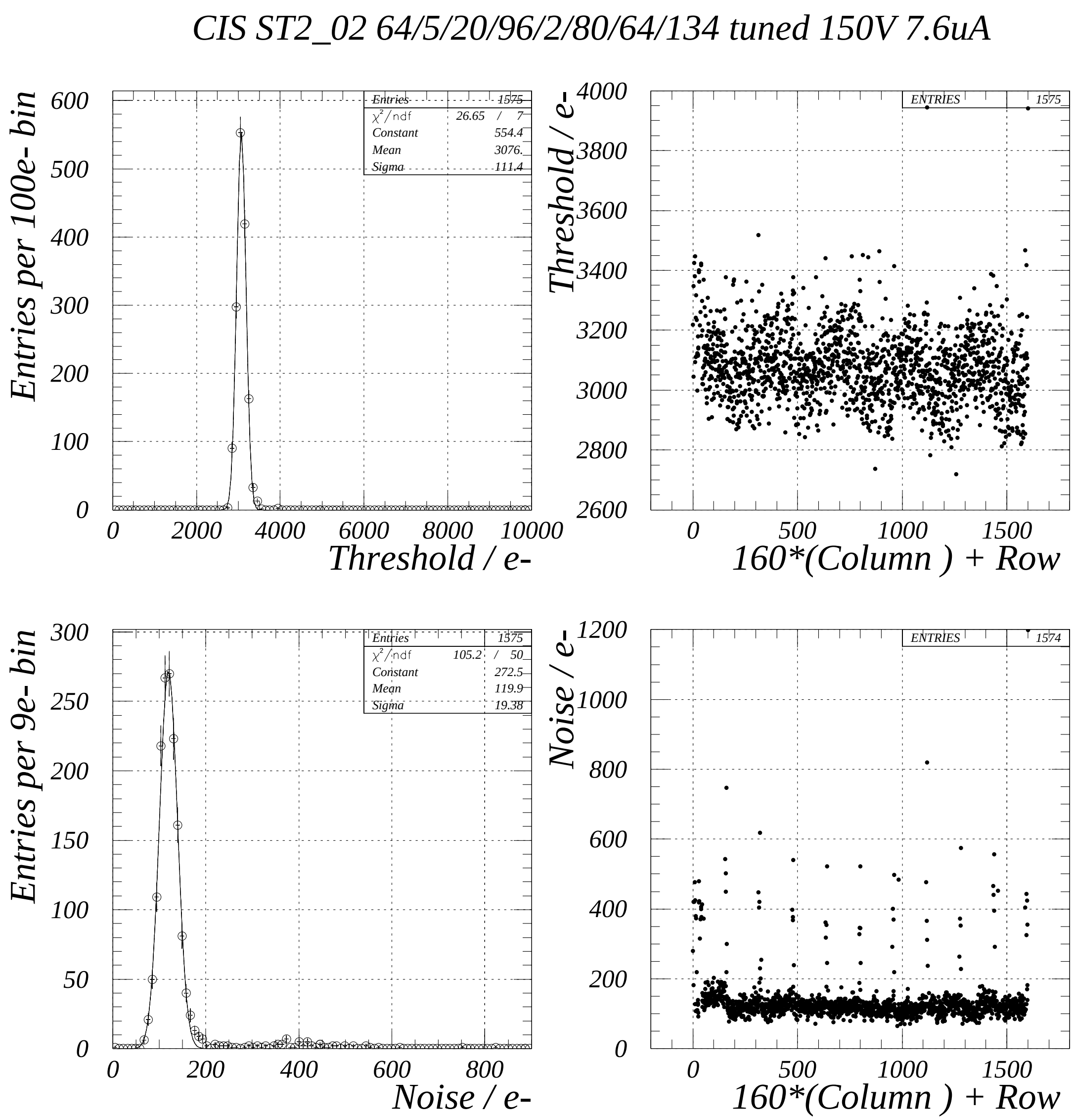
- Threshold = 2940e
- Dispersion = 190e
- Noise = 180e

- Standard TOT calibration for the same conditions:



- With this feedback current, MIP eak is at about 20 counts

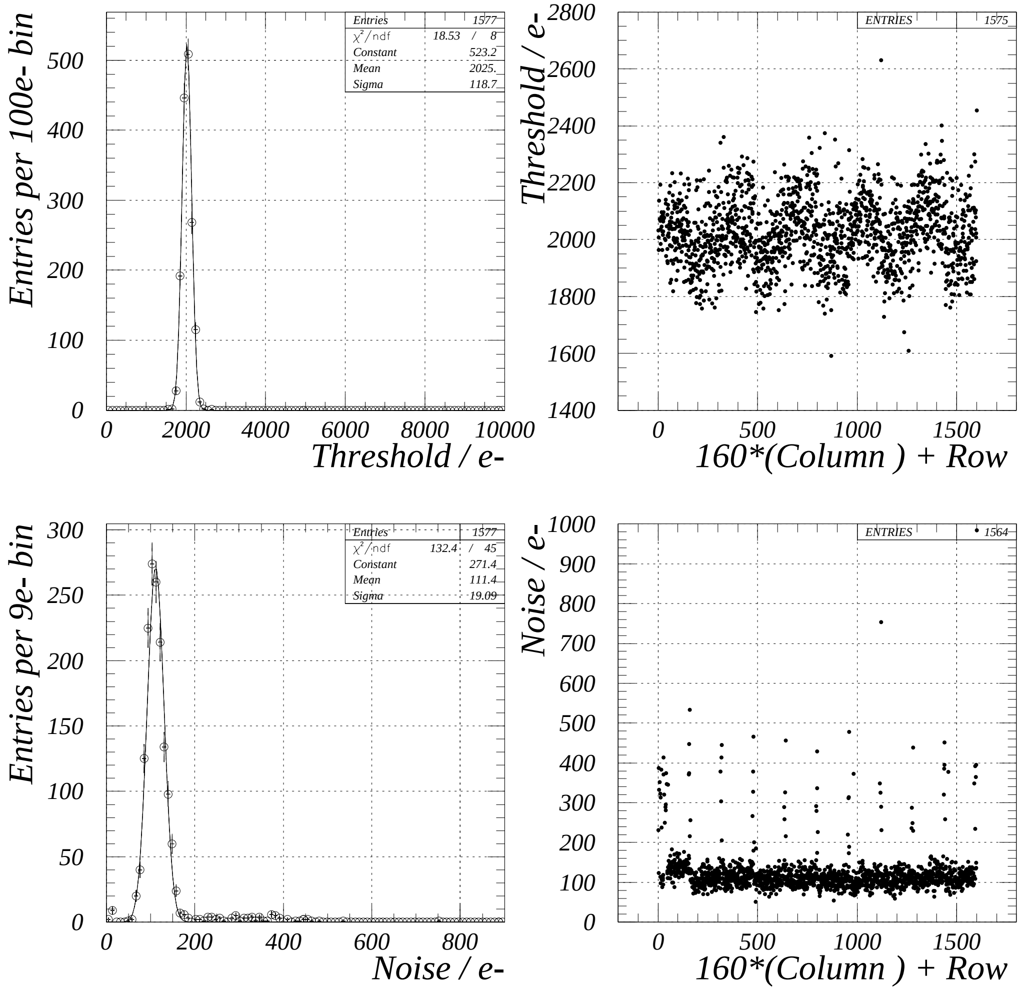
- Have developed operating point with low feedback current to reduce noise, reduce threshold dispersion, and increase resolution of charge measurement.



- Dispersion reduced to 110e for same threshold
- Noise reduced to 120e

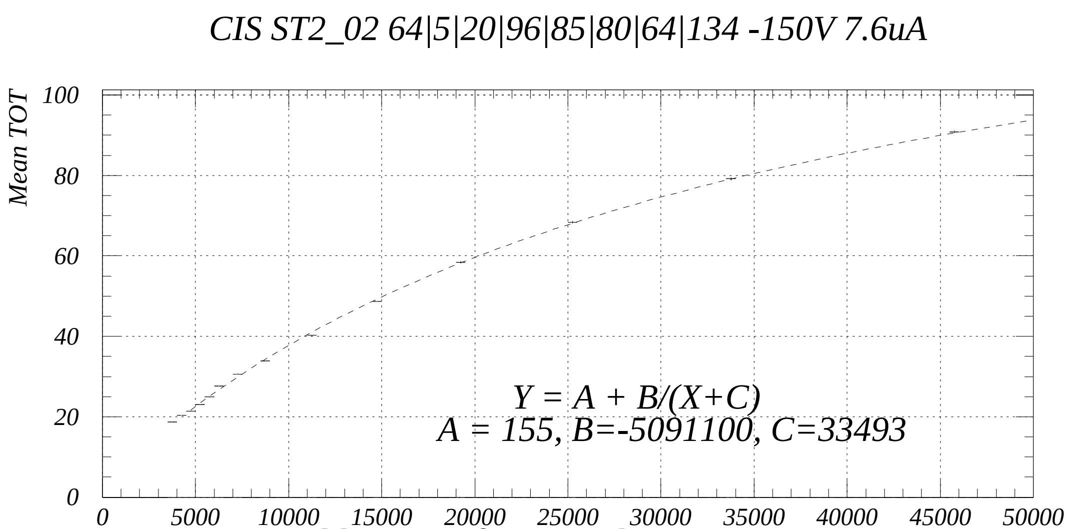
- Using this configuration, one can reach thresholds of 2000e or less:.

CIS ST2_02 64/5/20/96/85/80/64/134 tuned 150V 7.6uA

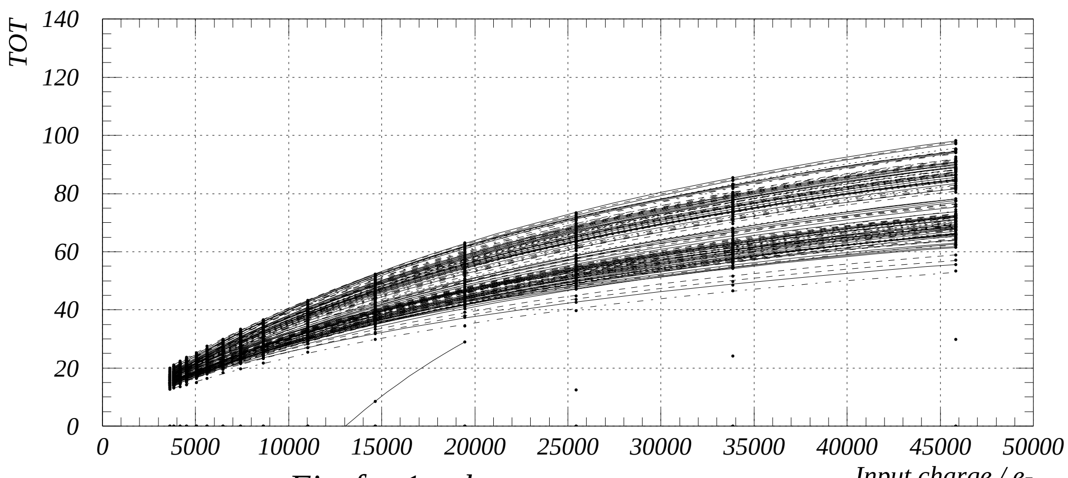


- ST2-02 (CIS-1M)
- Threshold = 2025e
- Dispersion = 120e
- Noise = 110e

- TOT calibration for this operating point:



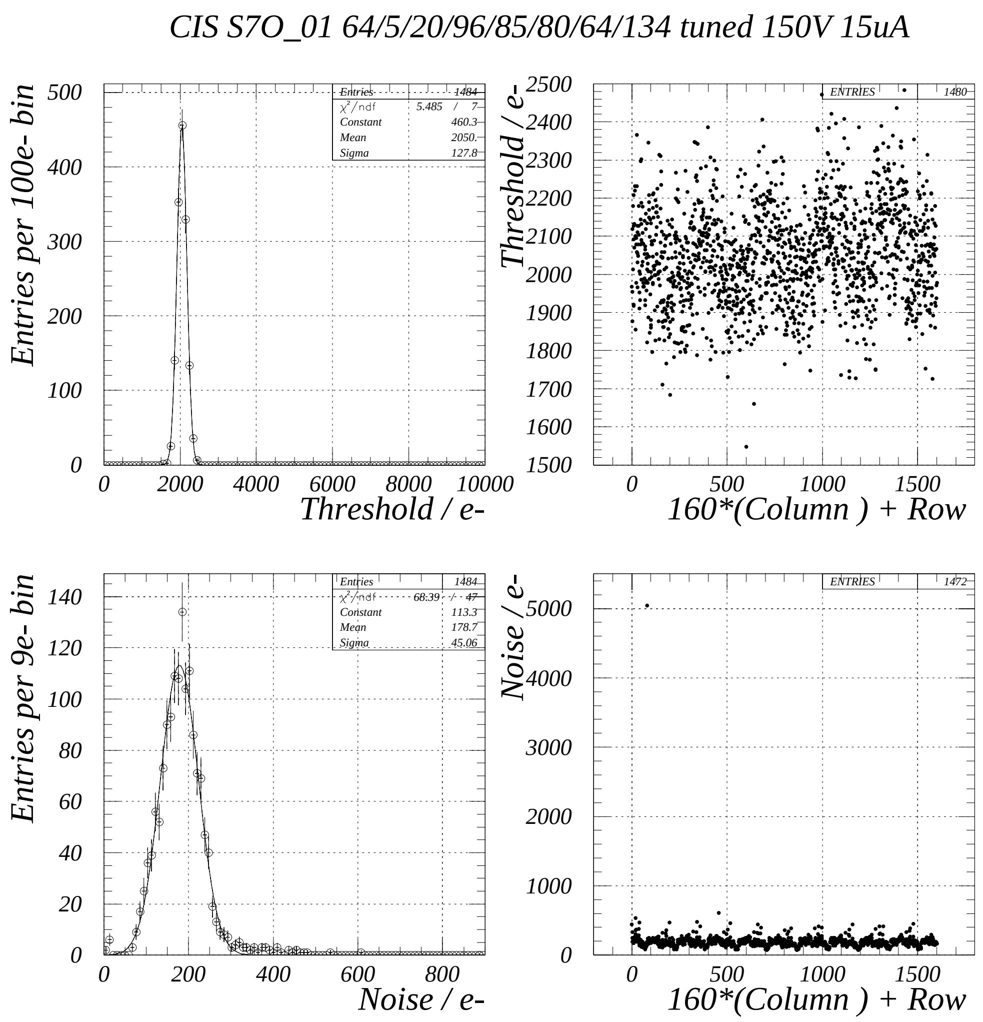
Mean calibration - first 10 columns



Fits for 1 column

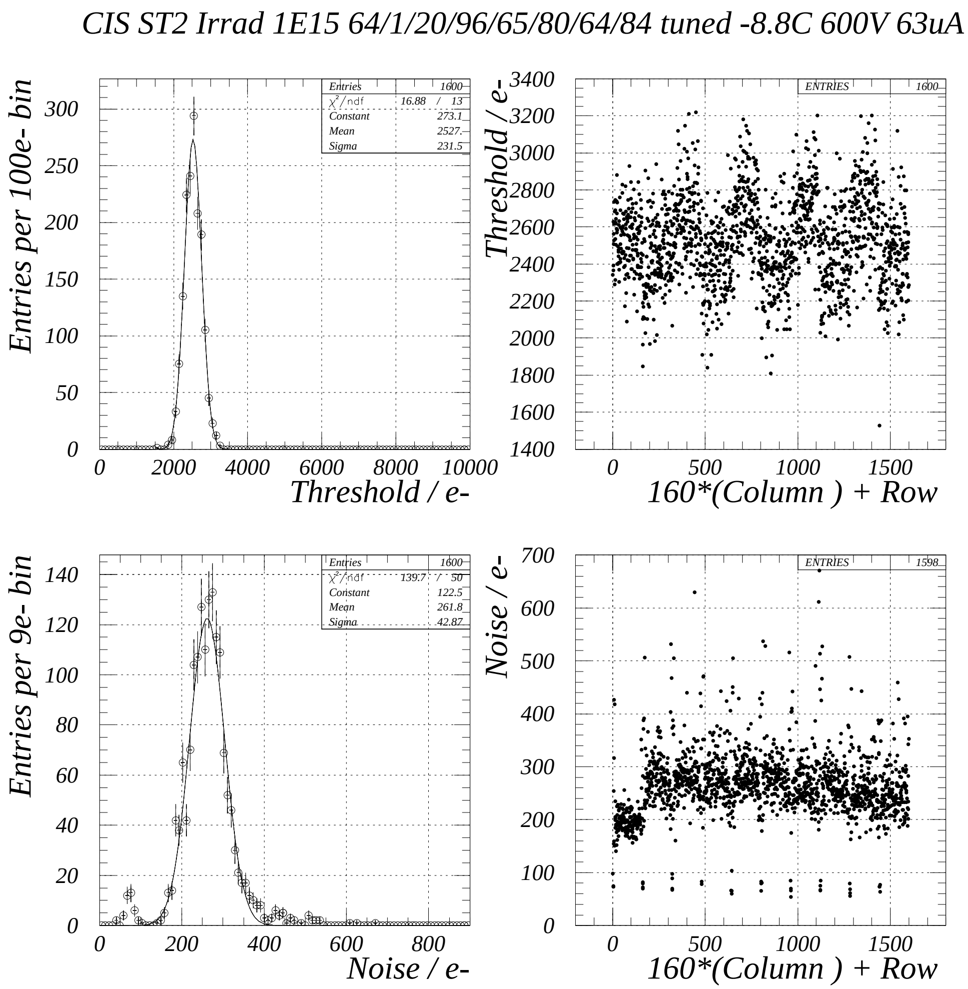
- Expected MIP peak appears at about 50-60 counts for this feedback current.
- Large odd/even row number dispersion is clear.
- Danger: some channels with large charges can fluctuate beyond L1

- Second of 4 detectors tuned for this low threshold (others look similar):



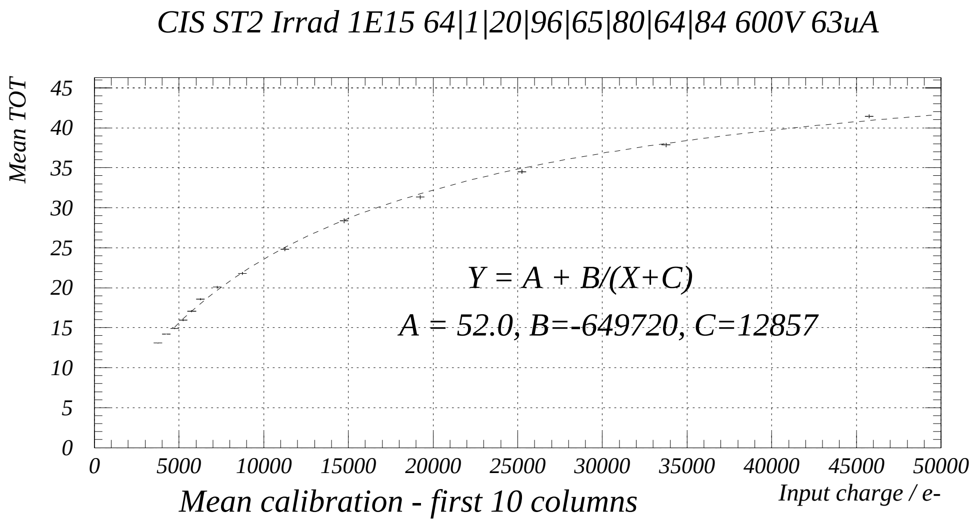
- Threshold = 2050e
- Dispersion = 130e
- Noise = 180e (many different detector designs, some with significantly higher noise than ST2 design)

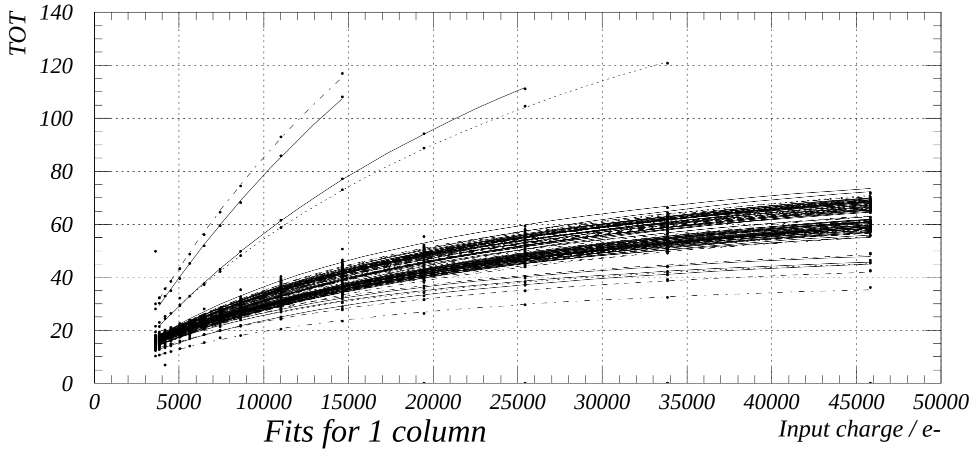
- Have characterized detectors irradiated to 10^{15} dose (leakage of 25 nA/pixel).



- ST2 Irradiated and biassed to -600V and operated at about -10 C
- Threshold 2500e
- Dispersion = 230e
- Noise = 260e (roughly as expected given shaping time and large leakage current).
- ATLAS spec: noise and dispersion in quadrature less than 400e (350e seen here).
- Minimal feedback current used to give best charge resolution

- TOT calibration for this detector

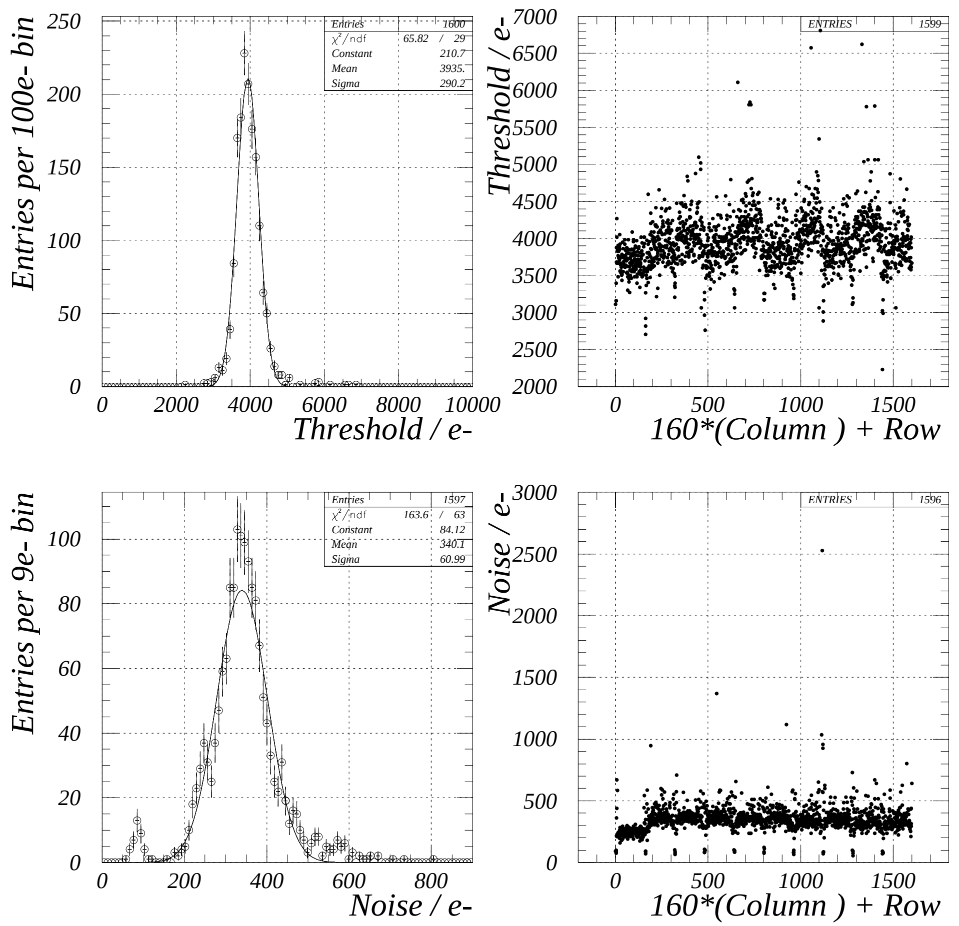




- Expected depletion voltage about 1200V. Operation at 600V should give 70% depletion.
- Dortmund charge prediction is about 7.5 Ke (I would have expected about 10 Ke ?)

- Same detector operated at higher temperature to double leakage current (about 50 nA/pixel):

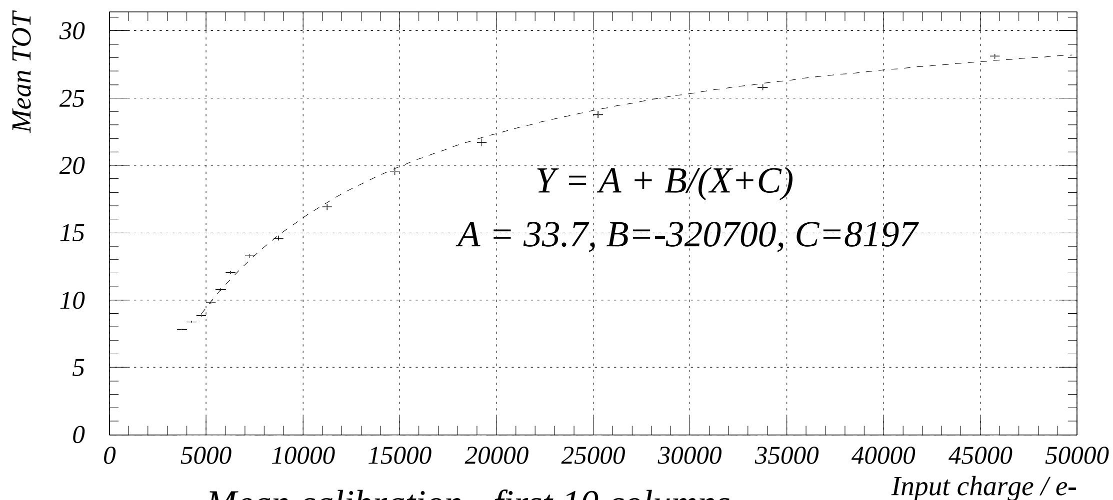
CIS ST2 Irrad 1E15 64/1/20/96/2/80/64/84 tuned -1.5C 500V 153uA



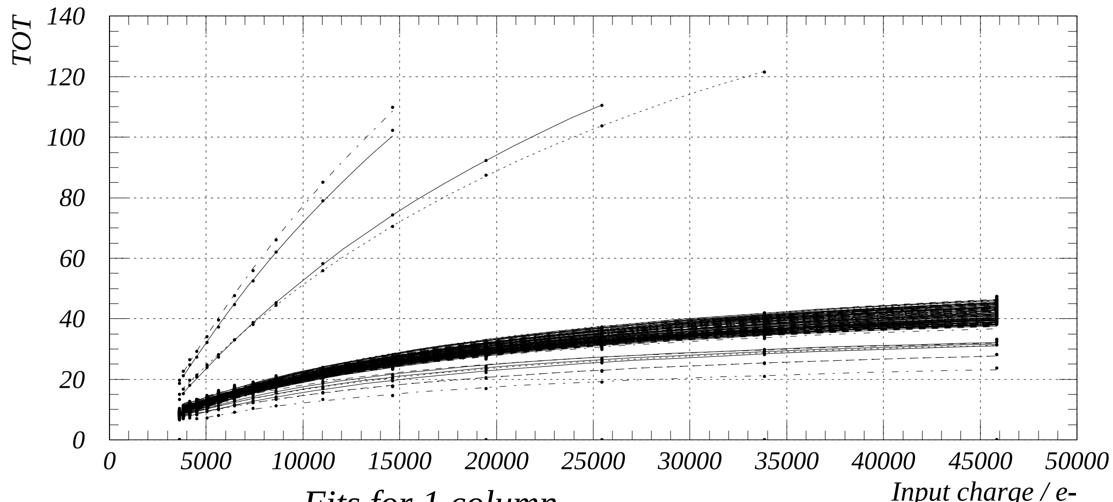
- Total leakage about 150 µA at -600V
- Threshold = 3900e, increases for same DAC settings due to larger leakage current (stronger shaping).
- Dispersion = 290e
- Noise = 340e
- Quadrature sum is about 450e, so could probably have operated this detector at 3000e threshold.

- TOT calibration with larger leakage current:

CIS ST2 Irrad 1E15 64|1|20|96|2|80|64|84 -1.5C -600V 153uA



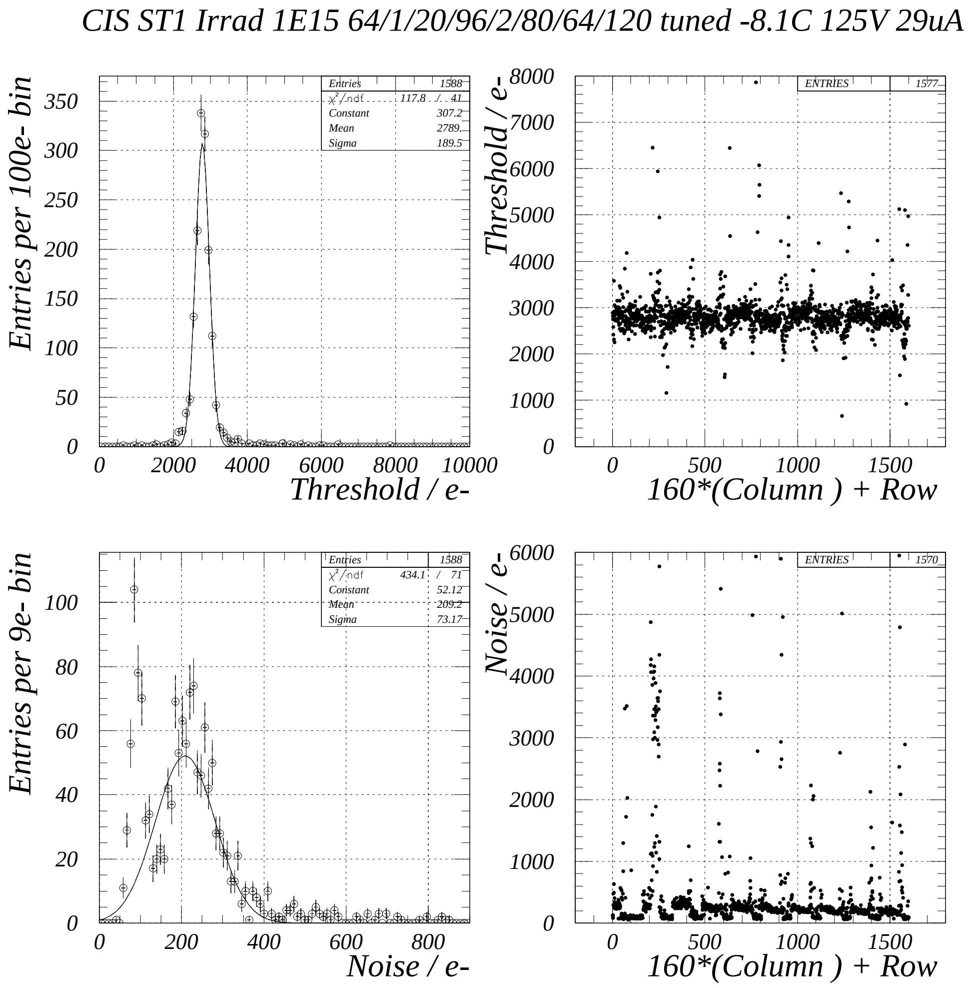
Mean calibration - first 10 columns



Fits for 1 column

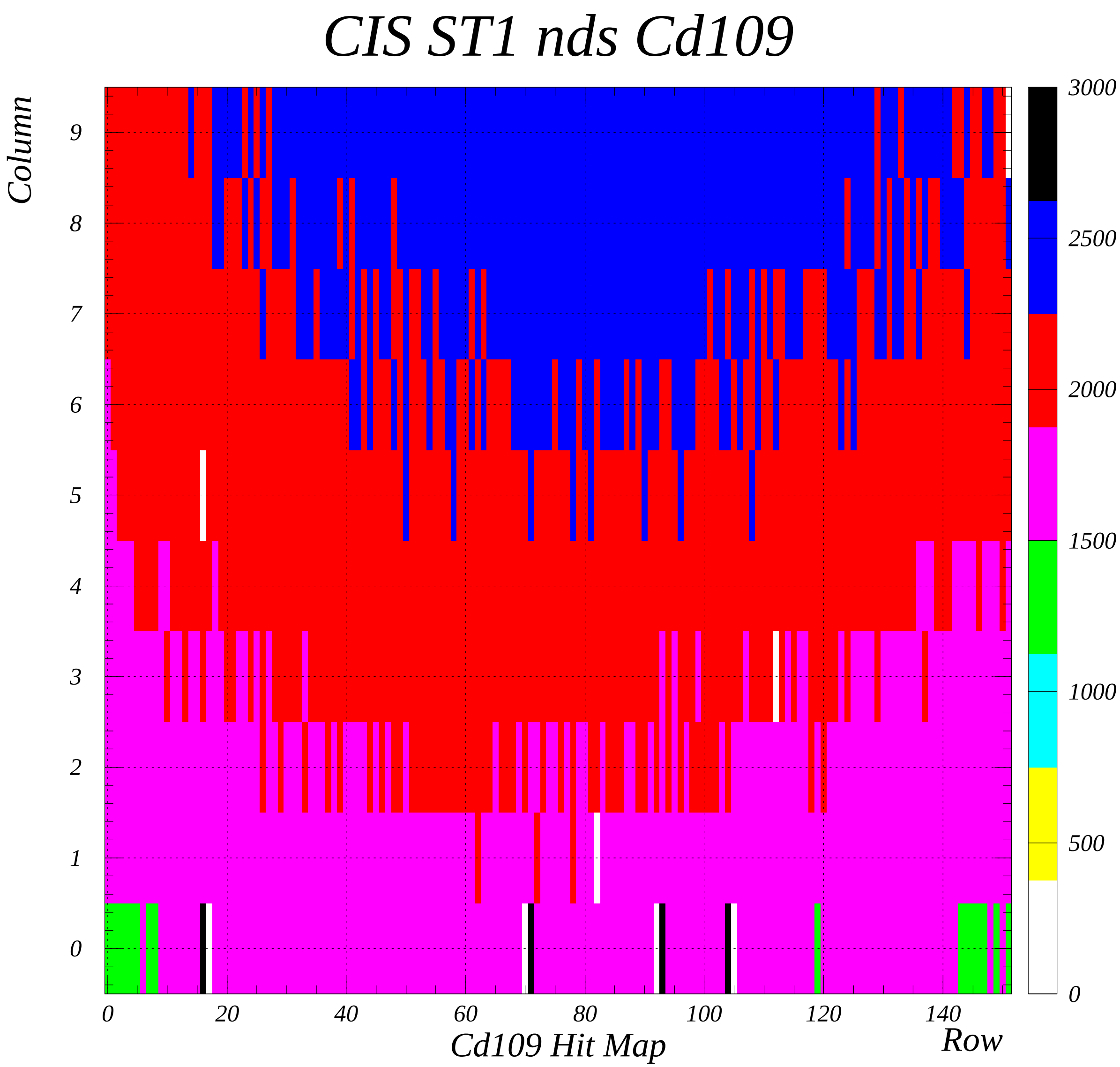
- Even with minimum feedback, there is not very much TOT information left at this leakage.

• ST1 detector irradiated to 10^{15} fluence:



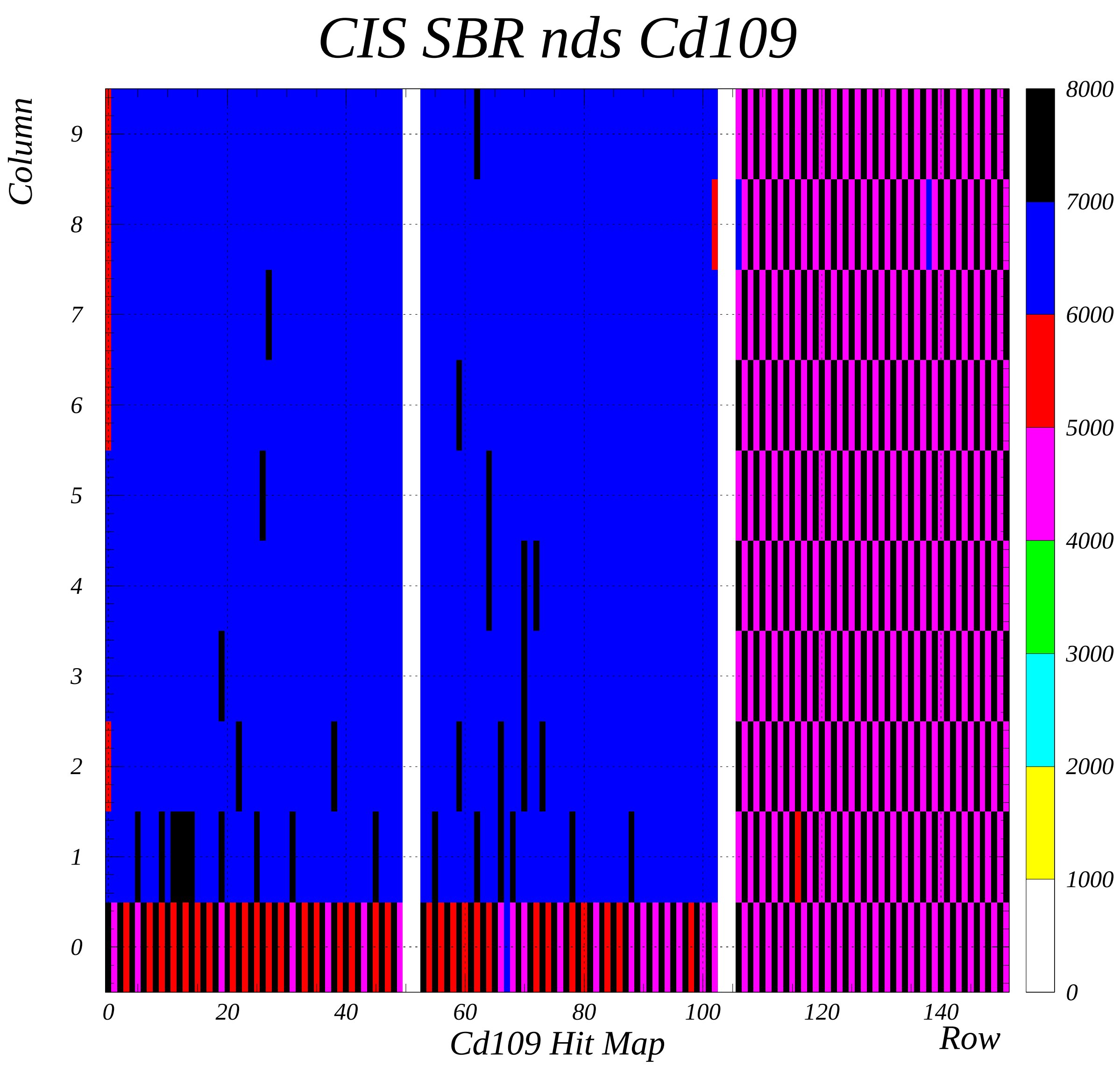
- Irradiated ST1 biassed to 125V (expected depletion voltage is about 1200V).
- Threshold = 2800e
- Noise = 210e, but many channels already have very large noise
- Extremely noisy operation in H8 environment, essentially not useful.
- In order to find quiet operation (no large regions of hot pixels), bias was even reduced to 10V. Some signals correlated with strips still observed.

- Source run (Cd109 = 1 fC) for detector running in Hitbus triggered mode:



- ST1 Detector operating at 3100e threshold
- Observe feature seen in many IZM detectors: dead channel next to channel which counts double (suggests shorted bumps)

- Source run for Bricked Detector SBR-01 (CIS-2M):



- Observe complex detector patterning:
- Upper region is "partially bricked" with alternating 300µ and 500µ pixels.
- Edge regions are partially bricked
- Other regions use 400µ pixels in true bricked geometry

Next steps for single chip studies:

- After recent testbeam and lab studies, would claim that if we can get the same level of performance from rad-hard chips that we now see in the rad-soft chips, we will meet our goals for ATLAS...
- We will continue to complete our systematic survey of the 29 assemblies. We have reached the stage where we should be able to account for the problems we see in every single assembly, to begin to understand yield and production issues.
- There are further assemblies being prepared with Alenia, both irradiated and un-irradiated, so these will also need to be characterized.
- Note: we have now assembled a total of 60 single-chip support cards, six of which will be for Alenia assemblies. We need to know what further needs there are so that more boards and parts can be ordered (this has been a lot of work and un-budgeted expense !)

We should define and organize remaining studies...

First results on Tile2 Module

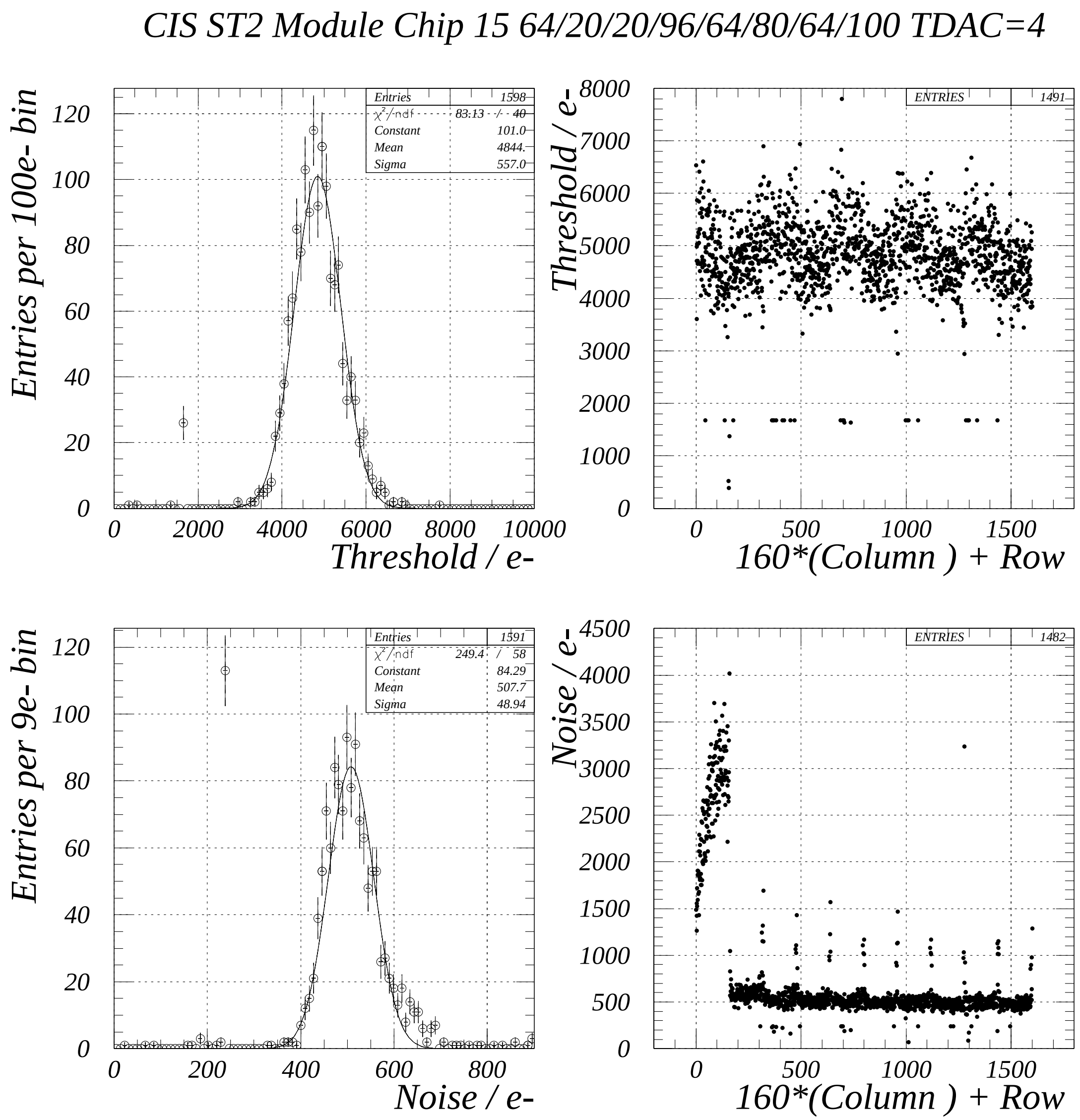
Module was flip-chipped in early June

- Emphasis has been on single chip assemblies so far.
- Have begun software work and studies to understand whether module is more or less than the sum of its parts.

Operating experience:

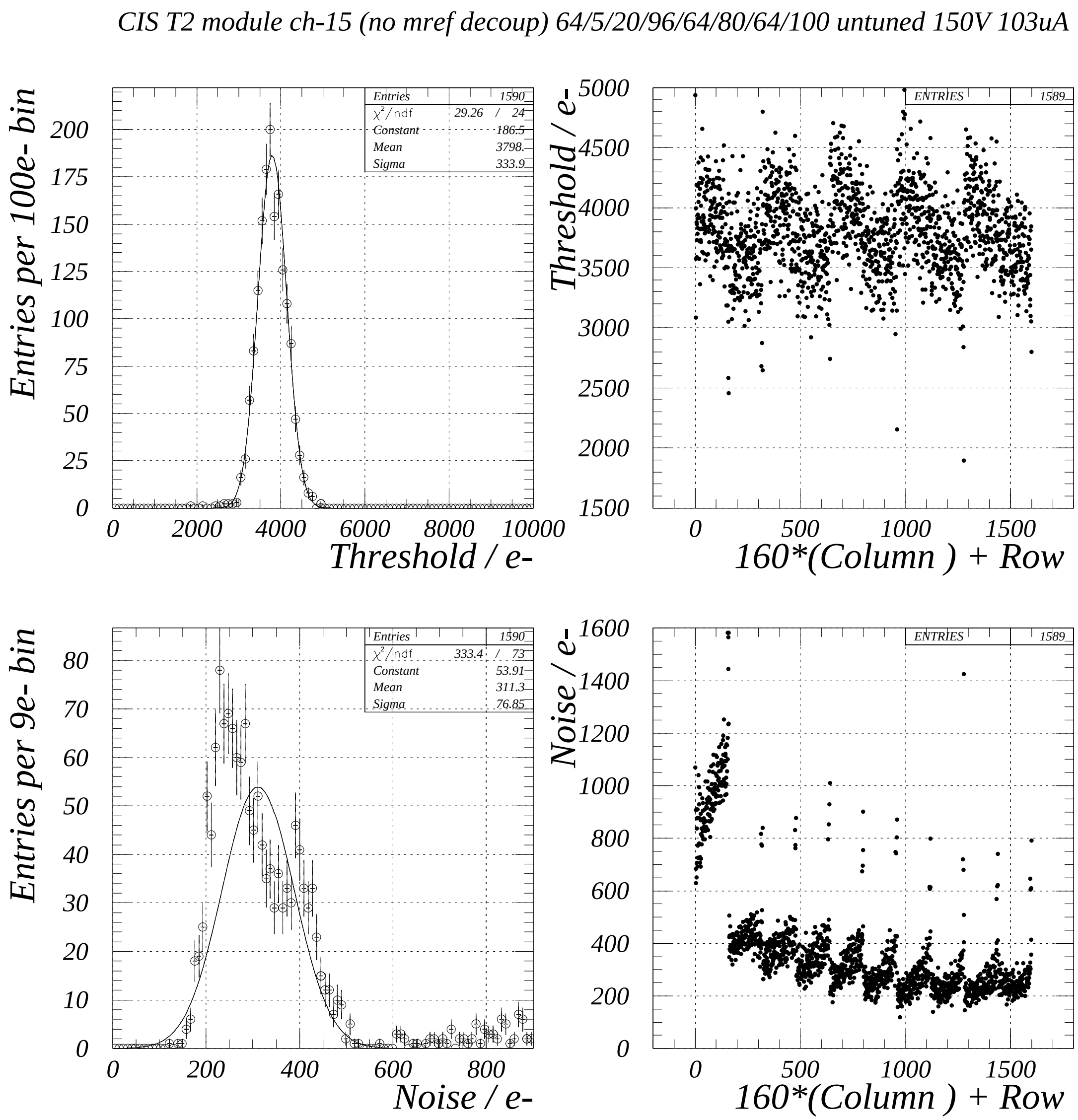
- Initially, thought detector was bad because it requires 100 mA to reach nominal -150V operating point. However, this just seems to be a feature of many Tile 2 detectors (so series resistor was reduced to 10K for further studies).
- One of 16 chips (number 8) has peculiar problem with serial data output, suggesting a problem with XCK (not yet investigated with Pico-probing). All registers operate normally for all chips, and all of the other 15 chips operate perfectly with digital injection.
- Analog charge injection works, but observe what appear to be significant bad regions on one side of the module (chips 0-7). Bad region typically appears in middle of leftmost columns, and is consistent between charge injection and Cd109 source measurements. Chips on the other side of the module look fine.
- Cd109 source studies of several chips look good, so detector and electronics seem to basically work.

- Typical threshold scan for module:



- Observe reasonable threshold behavior (external injection via Siegen PCC used here since FE-B internal chopper behaves badly for threshold scans).
- Noise behavior is very poor. For this feedback current, expect about 200e noise on Tile 2
- Poor behavior in Column 0 (600µ pixels to cover overlap)

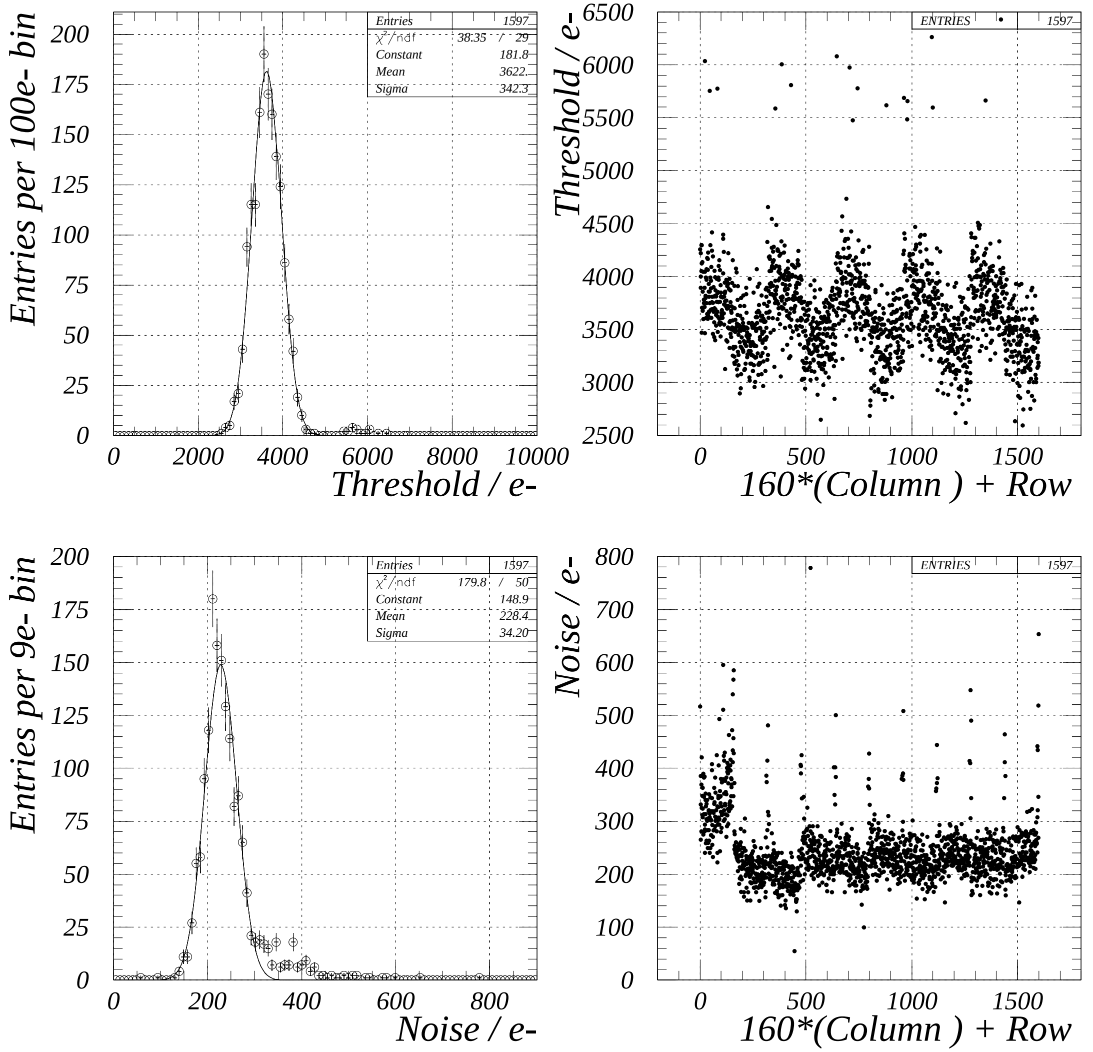
- Scan of same chip after removing MON_REF wirebond:



- Observe significant noise improvement after this change ?
- Module support card has much longer traces from the sensitive analog nodes to the decoupling than single chip support card, and these capacitors also provide a mechanism for noise injection.

- Threshold scan on neighboring chip after removing 8 IBias decoupling capacitors (initial scan looked the same as for chip 15):

CIS T2 module chip-14 (no decoupling) 64/5/20/96/64/80/64/100 untuned 150V 103uA



- Very significant improvement observed.
- Clearly, further study of grounding and decoupling is needed for module.
- Will try to do this systematically...

Next steps for modules:

- Second module, using Seiko Tile 1 detector, is now being bonded. Similar studies will be carried out for this module.
- Third module has been flipped by Boeing for prototype studies with flex hybrid.
- Fourth module, using thinned chips (150μ) ready for flip-chipping at Boeing (see Gil's talk for details).

Strongly suggest that further module construction take place as soon as possible:

- Would like to get at least one IZM module with FE-B (preferably a Tile 2).
- Now that FE-C works well, should build a module at IZM using these chips.
- There will be 1-2 MCM-D modules made at IZM (number and schedule ?)

Studies so far have used MCC replacement chip.

- Clearly a next step is to read out complete module with MCC and see if there are additional electrical issues.

We urgently need to understand module system issues before submitting next generation FE chips !